adjusts a phase of the second clock such as to fix relative phase difference between the phase adjustment signal and the first clock, wherein

said semiconductor device is a semiconductor memory device including an output buffer from which data stored in memory cells is output in synchronism with the second clock.

4. (Amended) A module comprising:

semiconductor devices;

a phase adjustment circuit generating a second clock so that a phase adjustment signal output from a first semiconductor device that is one of the semiconductor devices and a first clock have a predetermined phase relationship, the second clock being supplied to the semiconductor devices; and

a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted,

the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a phase of the second clock such as to fix a relative phase difference between the phase adjustment signal and the first clock, wherein

each of said semiconductor devices is a semiconductor memory device including an output buffer from which data in memory cells is output in synchronism with the second clock.

5. (Amended) The module as claimed in claim 4, wherein the module comprises first data lines over which data output from the semiconductor devices are transferred, and a second data line over which the phase adjustment signal output from

the first semiconductor device is transferred,

the first and second data lines being provided on the wiring board.

15. (Amended) The module as claimed in claim 4, further comprising a terminal that is provided on the wiring board and is used to output the phase adjustment signal to an outside of the module.

16. (Amended) The module as claimed in claim 4, wherein the first semiconductor device generates the phase adjustment signal in accordance with a predetermined signal given from an outside of the first semiconductor device.

17. (Amended) The module as claimed in claim 4, wherein:

the semiconductor devices including the first semiconductor device have an identical circuit configuration; and

the first semiconductor device has an output circuit that receives an external instruction that instructs the first semiconductor device to generate the phase adjustment signal.

18. (Amended) The module as claimed in claim 4, wherein the first clock is supplied from an outside of the module.

19. (Amended) The module as claimed in claim 4, further comprising a circuit generating the first clock from an external clock.

20. (Amended) The module as claimed in claim 4, wherein each of the semiconductor devices comprises a programmable delay circuit that delays the second clock.

21. (Amended) The module as claimed in claim 4, wherein the semiconductor devices comprise semiconductor memory devices.

22. (Amended) The module as claimed in claim 4, wherein the phase adjustment circuit generates the second clock from dummy output data output by the first semiconductor device.

23. (Amended) The module as claimed in claim 4, further comprising a second phase adjustment circuit generating a third clock so that the third clock and the first clock have a predetermined phase relationship, the third clock being supplied to the semiconductor devices.

25. (Twice Amended) A system comprising:

modules;

a wiring board on which the modules are mounted; and

a dummy output load line serving as loads of dummy output data output from the modules, wherein the modules comprise a module including;

a semiconductor devices, one of which is a first semiconductor device that outputs a phase adjustment signal;

a phase adjustment circuit which receives the phase adjustment signal output from said first semiconductor device and a first clock supplied from an exterior of said module, and generates a second clock, the second clock being supplied to the semiconductor devices; and

a wiring board on which the semiconductor devices and the phase adjustment circuit are mounted,

the first semiconductor device including an output circuit generating the phase adjustment signal from the second clock, wherein said phase adjustment circuit adjusts a